IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Applicant:	§	
Arkadiy MORGENSHTEIN, et al	§	
Serial No.: 10/648,474	§	
Filed: August 27, 2003	§	Group Art Unit: 2819
For: Logic Circuit and Method of Logic Circuit Design	§	Attorney Docket: 26327
Examiner: Daniel D. Chang	§	

ELECTION

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

This is in response to the United States Patent and Trademark Office Restriction Action mailed December 16, 2004, which response is being made on or before January 16, 2005.

Applicants hereby elect Group I, namely Claims 1 – 46, drawn to a logic circuit.

Applicants reserve the right to file, at a later date, additional divisional applications claiming priority from the present application which are directed to any one or more of the non-elected Groups.

Respectfully submitted,

Sol Sheinbein
Registration No. 25,457

Date: January 10, 2005